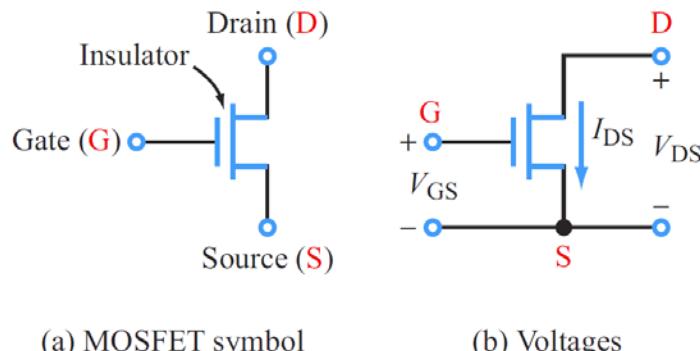


The Metal Oxide Semiconductor Field Effect Transistor (MOSFET)

Just as with the BJT, a complete of a MOSFET is well outside the scope of this class. However, a basic understanding of what happens in a MOSFET and an example of a simple model are provided below. For more information, several excellent texts exist for beginners, including *Fundamentals of Microelectronics* by Razavi and *The Art of Electronics* by Horowitz and Hill.

The simplest symbol for a MOSFET, which stands for metal-oxide semiconductor field-effect transistor, is shown below.



The vast majority of commercial computer processors are built with MOSFETs. A MOSFET has three terminals: the **gate (G)**, the **source (S)**, and the **drain (D)**. Actually, it has a fourth terminal, namely its **body (B)**, but we will ignore it for now because for many applications it is simply connected to the ground terminal. The circuit symbol for the MOSFET may look somewhat unusual, but it is actually a stylized depiction of the physical cross section of a real MOSFET. In a real MOSFET, the gate consists of a very thin layer ($< 500 \text{ nm}$ thick) of a conducting material adjacent to an even thinner layer ($< 100 \text{ nm}$) of insulator. The insulator in turn is placed directly on the surface of a relatively large slab of semiconductor material, usually referred to as "the chip" in everyday conversation (usually made of silicon 0.5 to 1.5 mm thick). The drain and the source sections are fabricated into this semiconductor chip on either side of the gate.

Note that because the gate G is separated from the rest of the transistor by the thin insulating layer, no current can flow from G to either D or S.

Nonetheless, it turns out that the voltage difference between terminals G and S is key to the operation of the MOSFET. Using terminal S as a reference above (right), we denote V_{DS} and V_{GS} as the voltages at terminals D and G, respectively. We also denote the current that flows through the MOSFET from D to S as I_{DS} . This simplification is justified by the assumption that no current flows through the gate node to either the drain or source node. The operation of the MOSFET can be analyzed by placing it in the simple circuit shown below, in which V_{DD} is a dc power supply voltage usually set at a level close to but not greater than, the maximum rated value of V_{DS} for the specific MOSFET model under consideration.

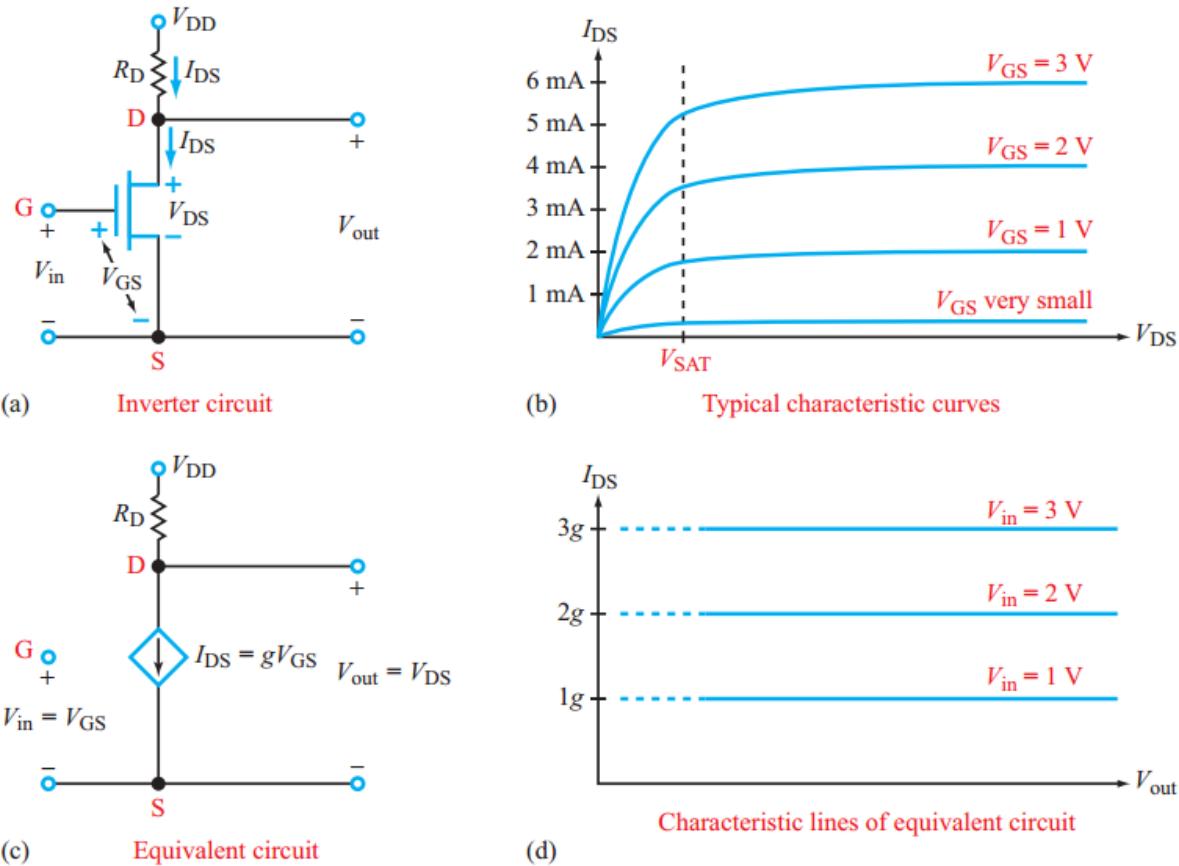


Figure 4-25: MOSFET (a) circuit, (b) characteristic curves, (c) equivalent circuit, and (d) associated characteristic lines.

$$I_{DS} = gV_{GS}, \quad (4.64)$$

The resistance R_D is external to the MOSFET, and its role will be discussed later. The input voltage is synonymous with V_{GS} and the output voltage is synonymous with V_{DS} .

Since current cannot flow from G to either D or S, the only current that can flow through the MOSFET is I_{DS} . The dependence of I_{DS} on V_{GS} and V_{DS} is shown for a typical MOSFET in Fig. 4-25(b) in the form of characteristic curves displaying the response of I_{DS} to V_{DS} at specific values of V_{GS} . We observe that if V_{DS} is greater than a certain saturation threshold value V_{SAT} , the curves assume approximately constant levels, and that these levels are approximately proportional to V_{GS} . These observations allow us to characterize the MOSFET in terms of the simple, equivalent circuit model shown in Fig. 4-25(c), which consists of a single dependent current source given by $I_{DS} = gV_{GS}$, (4.64) where g is a MOSFET gain constant. The characteristic curves associated with this model, which is valid only if V_{DS} exceeds V_{SAT} , are shown in Fig. 4-25(d).

In real MOSFETs, the relationship between I_{DS} and V_{GS} at saturation is not strictly linear. How linear the relationship depends (in part) on the size of the transistor. Modern sub-micron transistors used in digital processors exhibit a linear relationship between I_{DS} and V_{GS} at saturation, whereas larger MOSFETs used for power switching may behave nonlinearly. For our purposes, the simplification denoted by Eq. (4.64) will suffice.

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