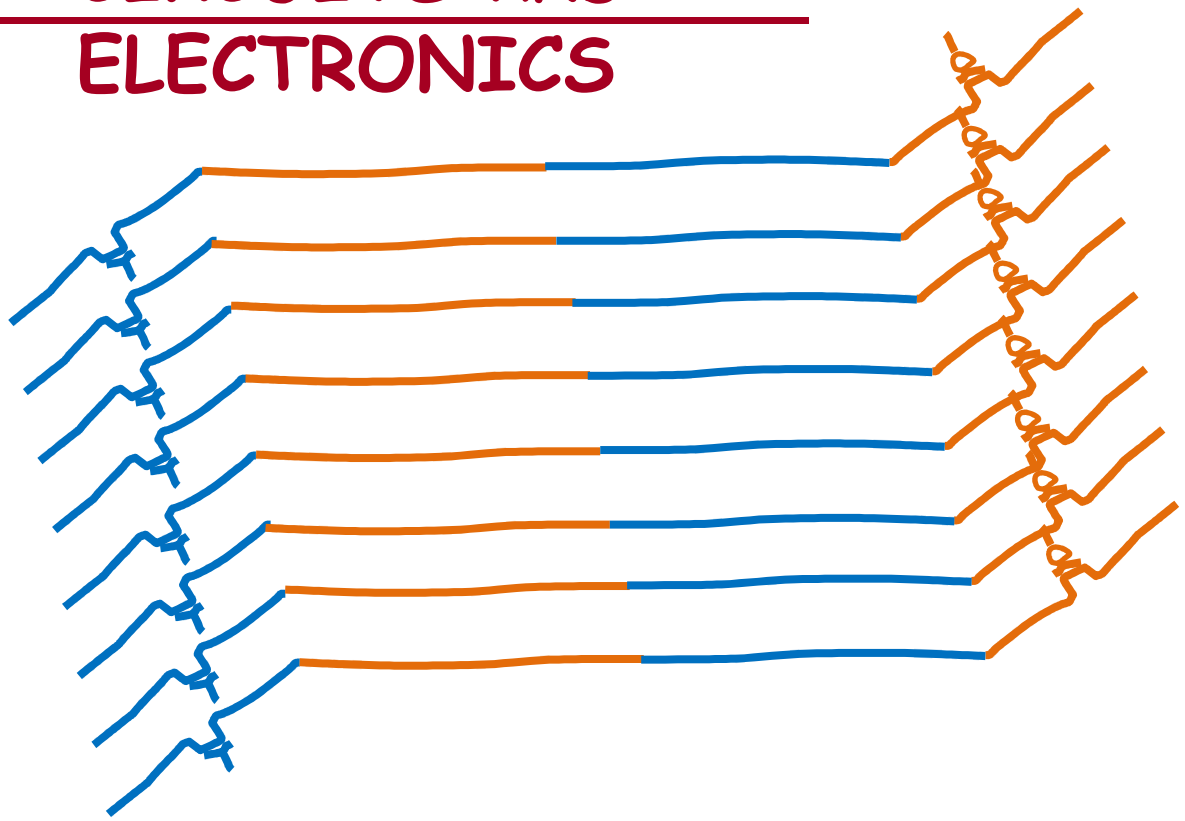
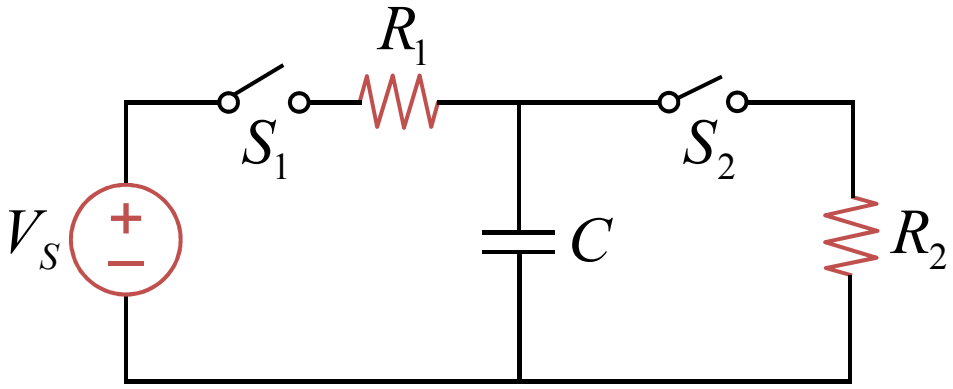
6.002x CIRCUITS AND ELECTRONICS

Energy, CMOS

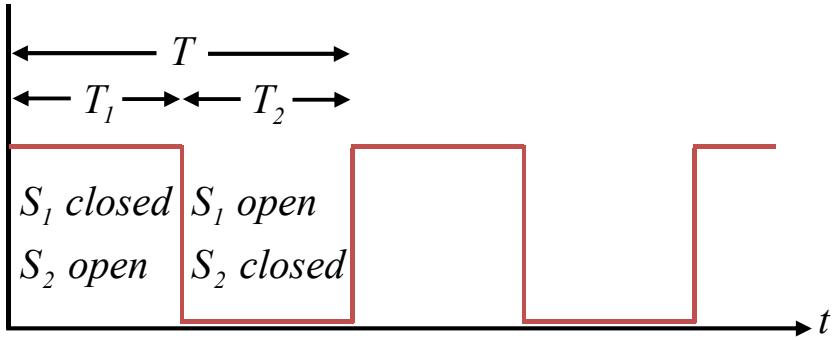


Reading Section 11.4, 11.5 of A&L

Review Hypothetical example circuit

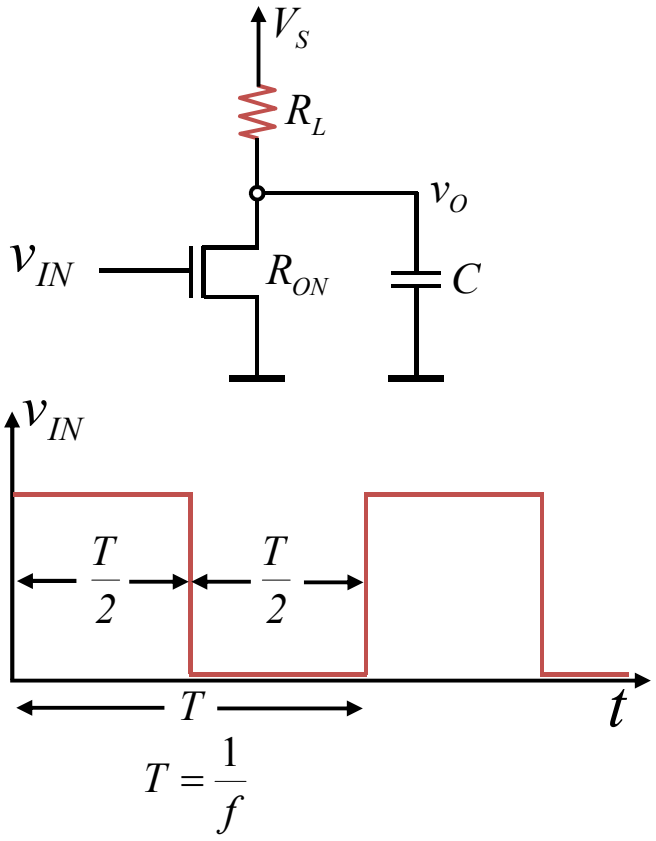


$$\overline{P} = CV_S^{\,2} f$$ ★★

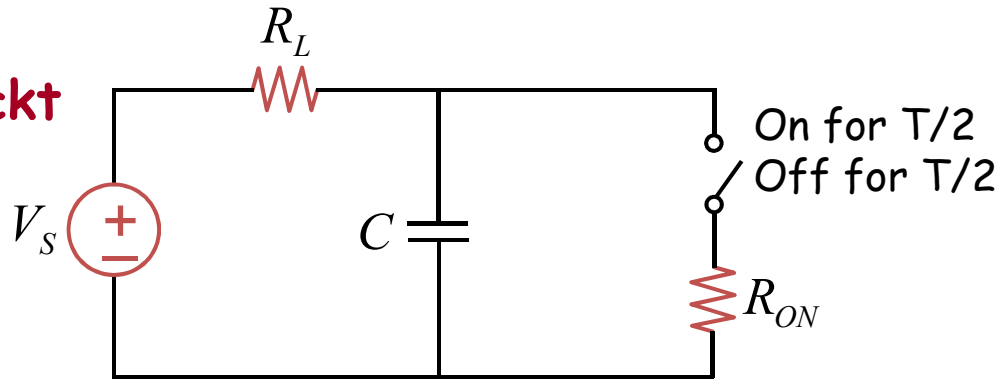


$$T = T_1 + T_2 = \frac{1}{f}$$

Review Inverter



Eqvt. ckt



$$\overline{P} = \frac{V_S^{\,2}}{2R_L} + CV_S^{\,2} f$$

$\overline{P}_{STATIC}$ $\overline{P}_{DYNAMIC}$

Review Inverter - numbers

One gate: $\overline{P} = \frac{V_S^2}{2R_L} + CV_S^2 f$

$C = 1f\,\mathrm{F}$

$R_L = 10\,\mathrm{k}\Omega$

$f = 3\times10^9$

$V_S = 5\,\mathrm{V}$

$\#\,\mathrm{gates} = 5\times10^6$

$$\overline{P} = 5\times10^6\left[\frac{25}{2\times10^4} + 10^{-15}\times25\times3\times10^9\right]$$

($\overline{P}_{STATIC}$ over the first term, $\overline{P}_{DYNAMIC}$ over the second)

$$= 5\times10^6\,[1.25\ \text{milliwatts} + 75\ \text{microwatts}]$$

6.25KW! — disaster!

375W — bad

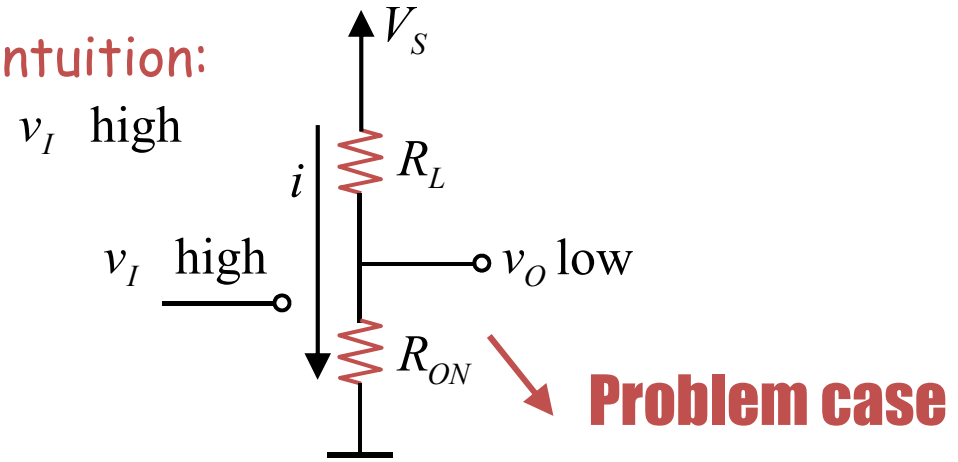
How do we get rid of static power?

How to get rid of static power

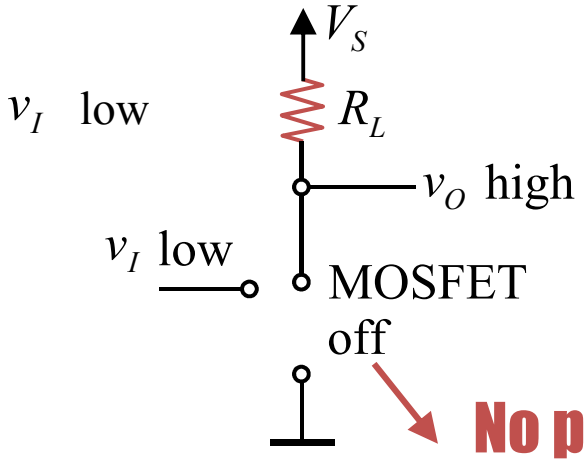
Intuition:

How to get rid of static power when input is high

Intuition:



Problem case

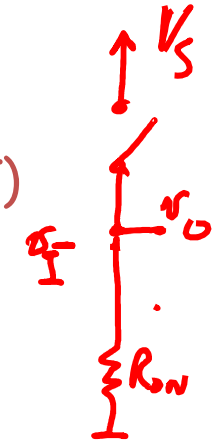


No problem

New Device PFET

N-channel MOSFET (NFET)

P-channel MOSFET (PFET)

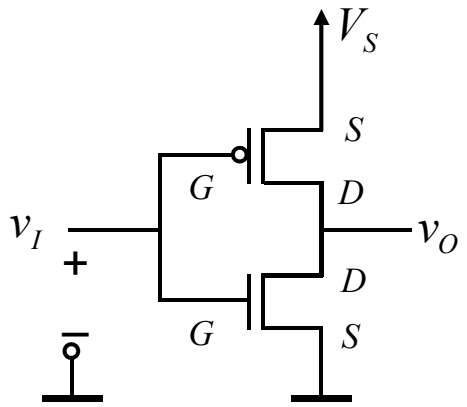


Consider this circuit

Behavior of the circuit

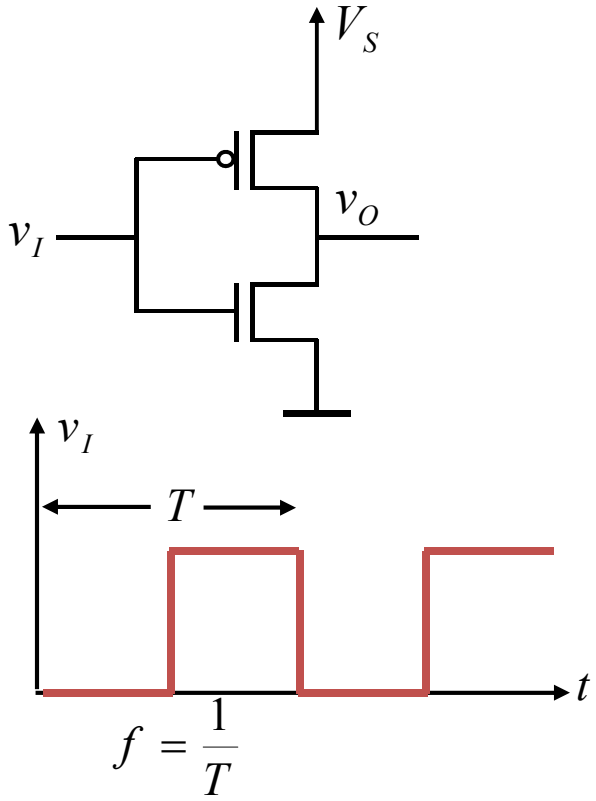
$v_I = 5V$ (input high)

$v_I = 0V$ (input low)



Key: no path from V_S to GND! no static power!

Let's compute $\overline{P}_{DYNAMIC}$



Using numbers from our previous example for CMOS

$$\overline{P} = CV_S{}^2 f$$

$$C = 1f\,\mathrm{F}$$

$$R_L = 10\,\mathrm{k}\Omega$$

$$f = 3\times 10^9$$

$$V_S = 5\,\mathrm{V}$$

$$\#\,\mathrm{gates} = 5\times 10^6$$

Scaling up

Increase frequency and number of gates, but if everything else stayed the same

Gates	f	$\overline{P}$
10^6	100 MHz	~2.5 watts
2×10^6	300 MHz	~15 watts
2×10^6	600 MHz	~30 watts
5×10^6	3 GHz	~375 watts
25×10^6	3 GHz	~1875 watts

$$\overline{P} = CV_S{}^2 f$$

$$C = 1f\,\mathrm{F}$$

$$R_L = 10\,\mathrm{k}\Omega$$

$$f = 3\times10^9$$

$$V_S = 5\,\mathrm{V}$$

How to reduce power

$$\overline{P} = CV_S{}^2 f$$

$$C = 1f\,\mathrm{F}$$

$$R_L = 10\,\mathrm{k}\Omega$$

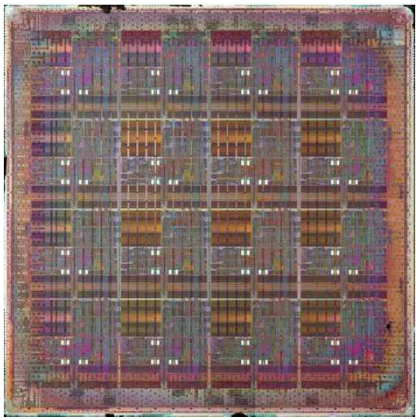
$$f = 3\times 10^9$$

$$V_S = 5\,\mathrm{V}$$

Real numbers

$$\overline{P} = CV_S^2 f$$

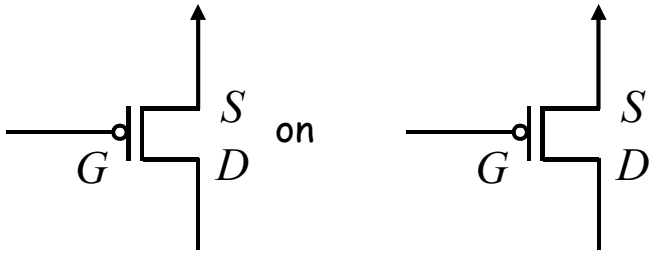
Transistors	f	$\overline{P}$	
2.5×10^6	66 MHz	15W	Intel Pentium 700nm, 1993
7.5×10^6	400 MHz	35W	Intel PII 350nm, 1997
44×10^6	1 GHz	15W	Intel PIII 180nm, 1999
120×10^6	0.43 GHz	18W	MIT Raw processor 16-core 180nm, 2002
120×10^6	3 GHz	75W	Intel PIV 130nm, 2001
615×10^6	0.7 GHz	20W	Tilera Tile64Pro 64-core 90nm, 2007
2300×10^6	3.6 GHz	75W	Intel Nehalem 8-core 45nm, 2011



http://groups.csail.mit.edu/cag/raw

Scaling up – leakage arises, causes static power dissipation

CMOS Logic



In general, if we want to implement F

If we want to implement F

