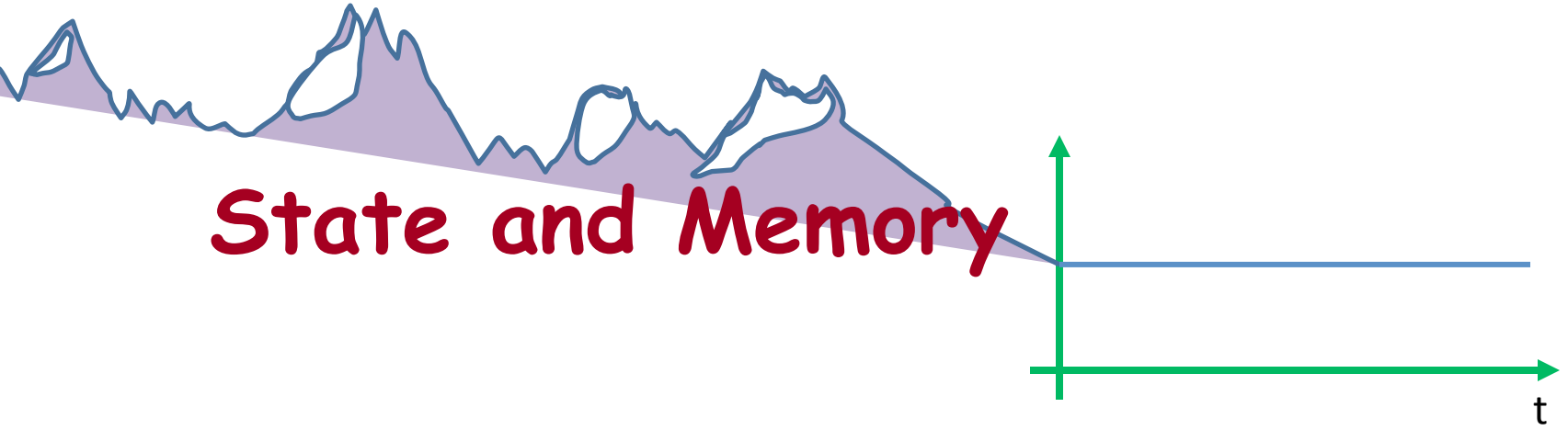
6.002x

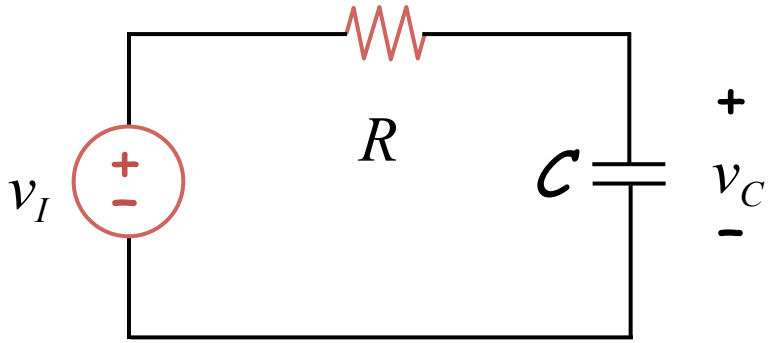
CIRCUITS AND ELECTRONICS



State and Memory

Review

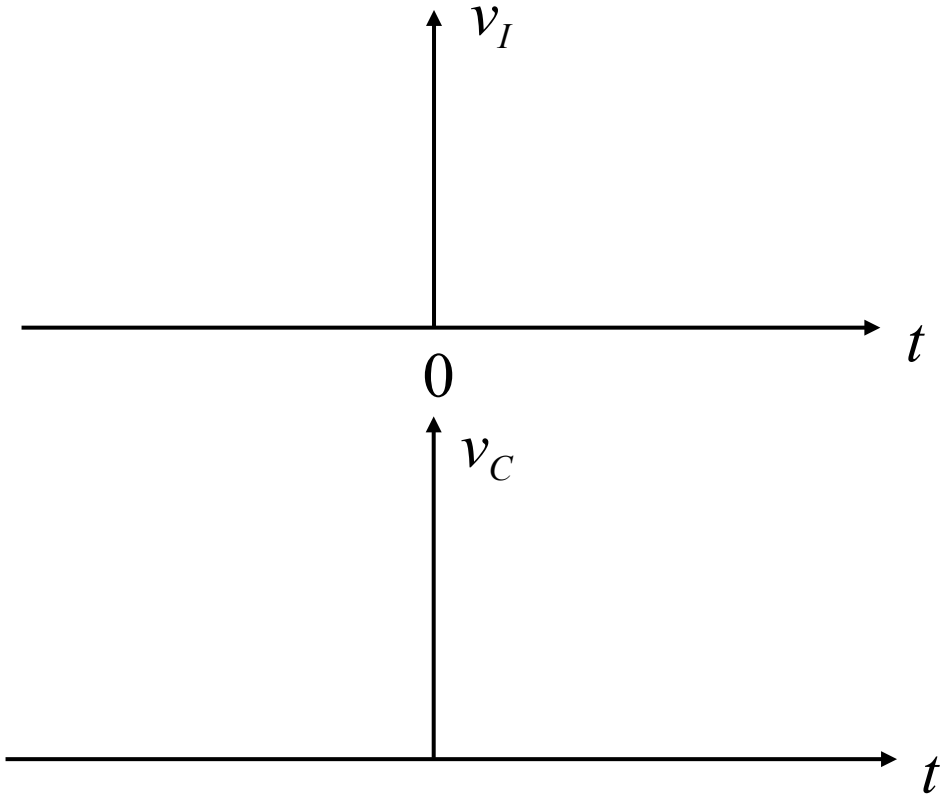
Recall



Reading: Section 10.3 and Chapter 11

This sequence will dwell on the memory property of capacitors

For the RC circuit in the previous slide



Notice that the capacitor voltage for t≥0 is independent of the form of the input voltage before t=0.

Instead, it depends only on the capacitor voltage at t=0, and the input voltage for t≥0.

State

State

ZIR and ZSR

We are often interested in circuit response for

One application of STATE ➡ DIGITAL MEMORY

Memory Abstraction

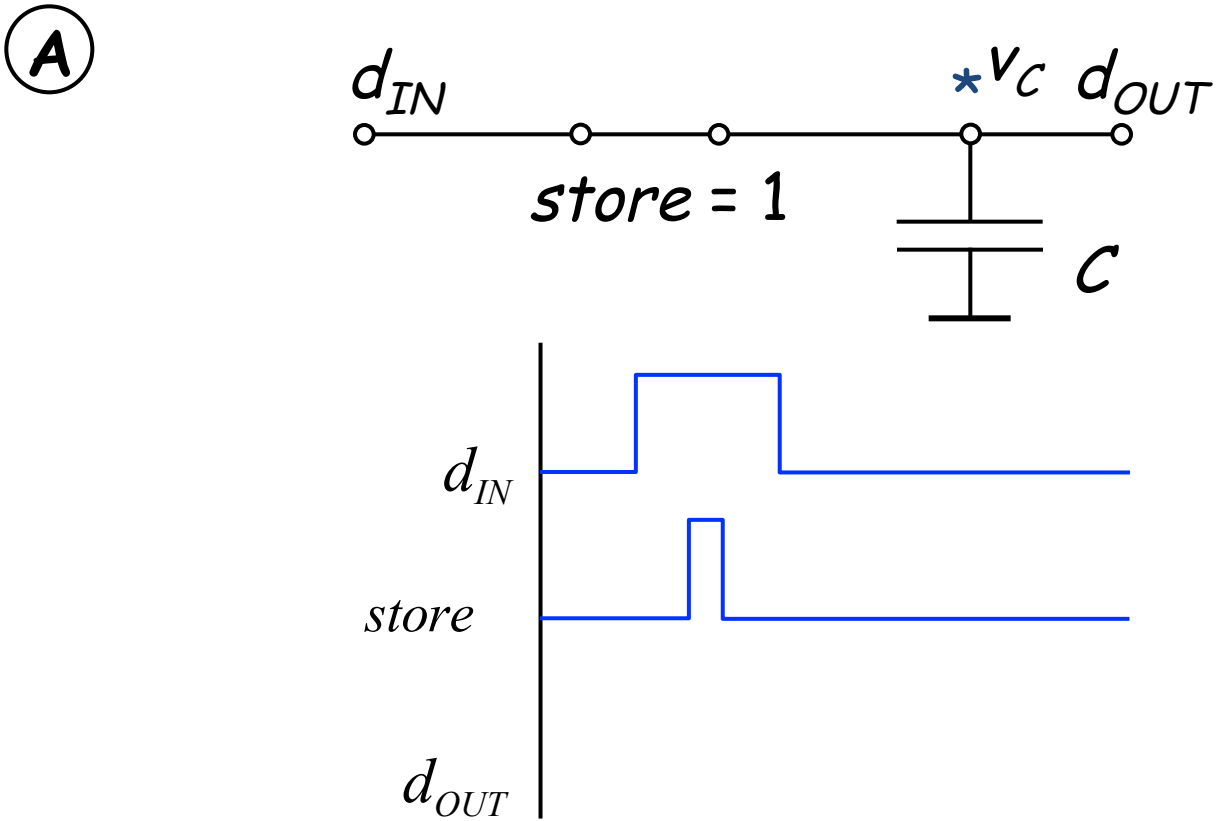
Remembers input when *store* goes high.

Like a camera that records input (d_{IN}) when the user presses the shutter release button.

The recorded value is visible at d_{OUT}.

Building a memory element …

Minimum store pulse width

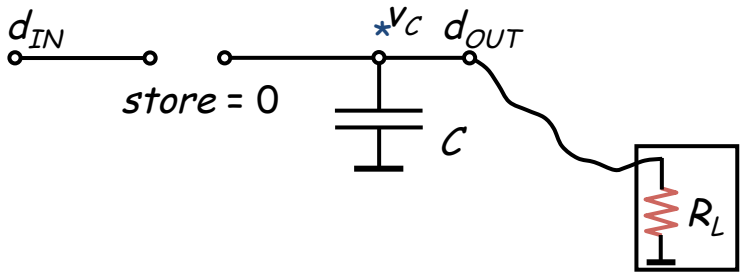


Storage time

Ⓐ

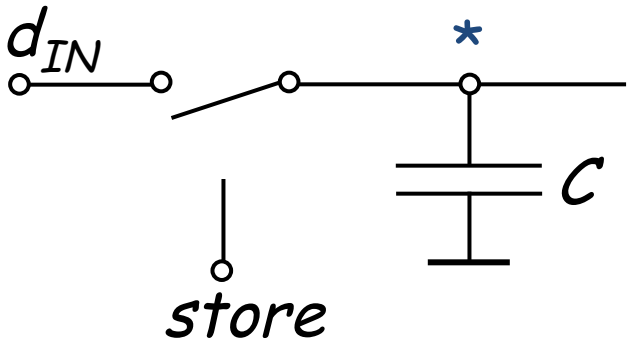
Storage time

Ⓐ



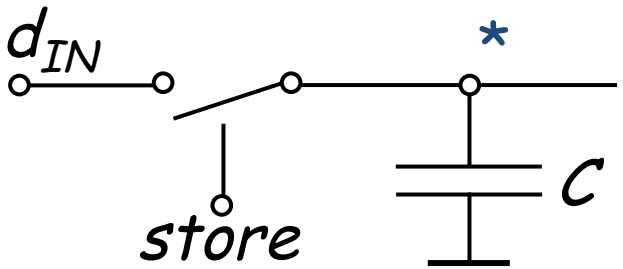
Building a memory element … second attempt

(B) Second attempt → buffer



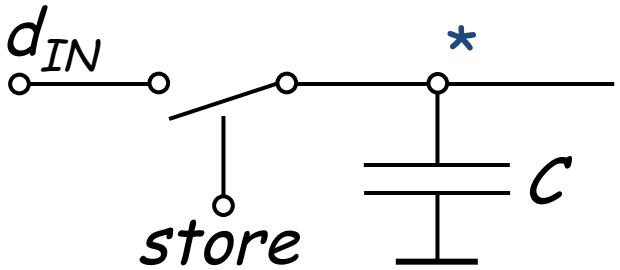
Building a memory element … buffer, refresh

Ⓒ Third attempt → buffer + refresh



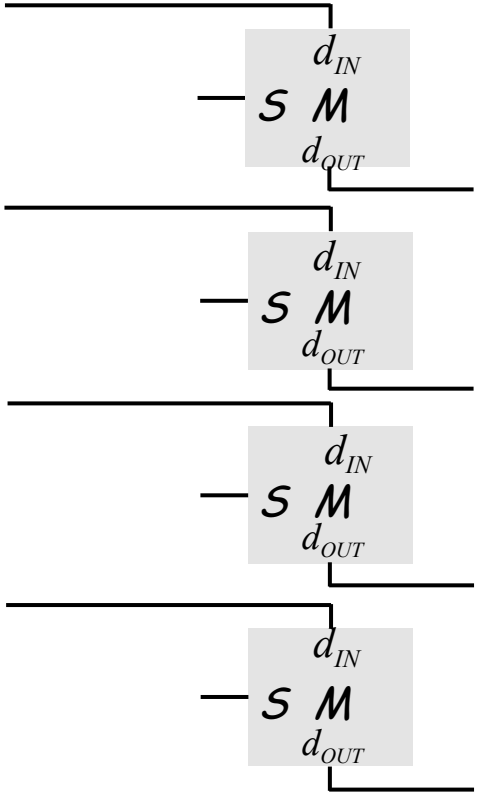
Building a memory element … buffer,decoupled refresh

Ⓓ Fourth attempt → buffer + decoupled refresh



A Memory Array

4-bit memory



Truth table for decoder

